Code No: 153AG

R18

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD
B. Tech II Year I Semester Examinations, April/May - 2023
COMPUTER ORGANIZATION AND ARCHITECTURE
(Common to CSE, CSBS, CSIT, CE(SE), CSE(CS), CSE(DS), CSE(N), AI&DS, AI&ML, CSD)

Time: 3 Hours **Max. Marks: 75**

Note: i) Question paper consists of Part A, Part B.
ii) Part A is compulsory, which carries 25 marks. In Part A, Answer all questions.
iii) In Part B, Answer any one question from each unit. Each question carries 10 marks and may have a, b as sub questions.

PART – A

(25 Marks)

1.a)	What is a computer?	[2]
b)	Explain functionalities of CPU.	[3]
c)	What are different addressing modes?	[2]
d)	Discuss about any two types of instruction formats.	[3]
e)	Give an example of decimal representation.	[2]
f)	Explain about BCD adder.	[3]
g)	What is magnetic tape?	[2]
h)	Describe parallel priority interrupt.	[3]
i)	What are conditions for incoherence?	[2]
j)	What are CISC characteristics?	[3]

PART – B

(50 Marks)

2.a)	Explain about computer design and architecture.	
b)	What are computer registers? Explain.	[5+5]
	OR	
3.a)	Discuss about shift microoperations in detail.	
b)	List and explain about memory-reference instructions.	[5+5]
4.a)	What are shift instructions? Explain with suitable examples.	
b)	Define control memory. Explain.	[5+5]
	OR	
5.a)	Explain about microinstruction format in detail.	
b)	What are RISC instructions? Explain.	[5+5]
6.a)	Discuss about complements in data representation.	
b)	Explain decimal arithmetic operations with examples.	[5+5]
	OR	
7.a)	Describe fixed-point representation in detail.	
b)	Discuss about division algorithms with examples.	[5+5]

8.a) Explain hardware organization and match logic of associative memory.
b) What are various modes of transfer? Explain. [5+5]

OR

9. Discuss about direct mapping and set associative mapping. [10]

10. Explain the following:
a) Interprocessor arbitration
b) Four-segment instruction pipeline. [5+5]

OR

11. Explain the following:
a) Interprocess communication and synchronization
b) Array processors. [5+5]

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